From Analog to Digital and Back Again

Joachim Hagenauer

Institute for Communications Engineering (LNT), Munich University of Technology (TUM), Munich, Germany

Abstract— In this tutorial talk the basic principles of analog decoders, equalizers and source decoders are explained. While the transmitter uses digital signal representation (i.e tailbiting convolutional and turbo codes) the receiver is realized as a fully analog circuit, allowing VLSI implementation at higher speed and less power consumption. A proof-ofconcept analog VLSI implementation is reported. As a case study a fully analog receiver for FEC-coded PCM signals is described.

Keywords— Analog Decoders, Analog VLSI, Turbo-Principle, Joint Source and Channel Decoding.

I. INTRODUCTION

In many areas source signals are still analog and the signals we send over transmission channels are also analog waveforms. For example, a cellular phone for speech accepts and transmits analog signals. Why going digital in between? There are good reasons for this of course, for instance we want to utilize the rich algebraic structure of error correcting coding. But we have already learnt that soft values used at the reveiver are better than binary values, and the success of 'turbo' decoding is due to the exchange of soft information between constituent decoders. Here we will describe highly parallel and nonlinear networks, performing the task of equalization, channel decoding and source reconstruction in a fully analog way. We will use in the analog networks turbo-feedback in several ways, but iterations are not discrete, but time continuous. These networks were first suggested in [Hag98b], [Loel98] and [HW98]. A broader introduction can be found in [HOMM99]. Performance is demonstrated by solving the network's non-linear differential equations and by already existing analog VLSI circuits (see [MGYH00]and [LUST99]). Such circuits use much less power at a higher speed than digital processors. Thus the borderline between analog and digital might shift in the analog direction.

II. ANALOG DECODERS IN VLSI

Using log-likelihood ratios(LLR) $L(x) = \frac{P(x=0)}{P(x=1)}$ of binary values x and soft-bits $\tanh(L(x)/2)$, the basics of analog decoders are described. The binary addition as used in parity check equations and in sub-trellises is represented by the so-called boxplus function involving nonlinear tanhelements. It turns out that LLR are represented by differential voltages in a VLSI circuit and the soft-bits by differential currents. The boxplus and summing elements are realized by nine-transistor circuit. From these elements the trellis is built up in hardware and performs the functions of an APP decoder with the BCJR algorithm. Especially decoding of tail-biting convolutional codes and turbo decoding fits well into this analog circuit setup. Extensions to equalizers and coded DPSK systems will be mentioned.

III. AN ALL ANALOG RECEIVER FOR CONVOLUTIONALLY ENCODED PCM SAMPLES

Analog networks for channel decoding can be further extended to source decoding, first proposed in [HOMM99]). Since our analog decoder produces soft outputs, we can get a slight performance improvement in source decoding using the analog output values or the 'soft' bits of the channel decoder instead of the hard decisions. As an example, PCM reconstruction based on the analog output of the channel decoder can also be implemented in an simple analog circuit. Hence, both analog techniques for channel decoding and source decoding can be integrated in one analog circuit.

We use here a samples of an correlated analog Gaussian source represented by PCM codewords and subsequently channel encoded with an overhead-free tailbiting convolutional code with unequal error protection. The fully analog receiver accepts the soft matched filter channel outputs and delivers the analog source signal. Turbo processing between the correlated source values and the analog tailbiting network decoder is included. Simulation results of the analog circuit show the expected performance and the feasibility of an analog VLSI implementation. No digital signal processing nor any D/A converter are required. Although the transmitter uses digital encoding (PCM and convolutional codes) the receiver is almost fully analog. Thus we perform a full swing from analog sources to digital coding and back to analog receivers.

References

- [Hag98b] Hagenauer, J., "Decoding of binary codes with analog networks," In: Proc. of the Information Theory Workshop 1998, San Diego, CA, USA, pp. 13-14, February 1998
- [Loel98] H.-A. Loeliger, M. Helfenstein, F. Lustenberger, and F. Tarkoey, "Iterative sum-product decoding with analog VLSI," in ISIT'98, Cambridge, MA, USA, p. 146, August 1998.
- in ISIT'98, Cambridge, MA, USA, p. 146, August 1998. [HW98] Hagenauer, J., Winklhofer, M., "The analog decoder," In: Proc. of Int. Symposium on Information Theory ISIT 1998, Cambridge, MA, USA, August 1998
- [HOMM99] J. Hagenauer, E. Offer, C. Méasson, and M. Mörz, "Decoding and equalization with analog non-linear networks," In European Transactions on Telecommunications (ETT), pp. 659– 680, November/Dezember 1999.
- [MGYH00] M. Moerz, T. Gabara, R. Yan, and J. Hagenauer, "An analog 0.25μm BiCMOS tailbiting MAP decoder," In Proc. IEEE International Solid-State Circuits Conference (ISSCC 2000), pp. 356-357, San Francisco, California, February 2000.
- [LUST99] F. Lustenberger, M. Helfenstein, H.-A. Loeliger, F. Tarköy, and G. S. Moschytz, "An analog decoding technique for digital codes," In Proc. of ISCAS '99, vol. II, pp. 428-431, Orlando, Florida, May/June 1999.

Invited Presentation at the 2001 Canadian Workshop on Information Theory, J. Hagenauer is with the Institute for Communications Engineering, Munich University of Technology, Germany. E-mail: J.Hagenauer@ei.tum.de.